

### FEATURES

**SNR = 75 dB,  $f_{IN}$  15 MHz, up to 105 MSPS**  
**SNR = 72 dB,  $f_{IN}$  200 MHz, up to 105 MSPS**  
**SFDR = 89 dBc,  $f_{IN}$  70 MHz, up to 105 MSPS**  
**100 dBFS multitone SFDR**  
**IF sampling to 200 MHz**  
**Sampling jitter 0.1 ps**  
**1.5 W power dissipation**  
**Differential analog inputs**  
**Pin compatible to AD6644**  
**Twos complement digital output format**  
**3.3 V CMOS compatible**  
**DataReady for output latching**

### APPLICATIONS

**Multichannel, multimode receivers**  
**Base station infrastructure**  
**AMPS, IS-136, CDMA, GSM, WCDMA**  
**Single channel digital receivers**  
**Antenna array processing**  
**Communications instrumentation**  
**Radar, infrared imaging**  
**Instrumentation**

### PRODUCT DESCRIPTION

The AD6645 is a high speed, high performance, monolithic 14-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on the chip to provide a complete conversion solution. The AD6645 provides CMOS-compatible digital outputs. It is the

fourth generation in a wideband ADC family, preceded by the [AD9042](#) (12-bit, 41 MSPS), the [AD6640](#) (12-bit, 65 MSPS, IF sampling), and the [AD6644](#) (14-bit, 40 MSPS/65 MSPS).

Designed for multichannel, multimode receivers, the AD6645 is part of Analog Devices, Inc. SoftCell® transceiver chipset. The AD6645 maintains 100 dB multitone, spurious-free dynamic range (SFDR) through the second Nyquist band. This breakthrough performance eases the burden placed on multimode digital receivers (software radios) that are typically limited by the ADC. Noise performance is exceptional; typical signal-to-noise ratio is 74.5 dB through the first Nyquist band.

The AD6645 is built on Analog Devices' extra fast complementary bipolar (XFCB) process and uses an innovative, multipass circuit architecture. Units are available in a thermally enhanced 52-lead PowerQuad 4 (LQFP\_PQ4) package specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  at 80 MSPS and  $-10^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  at 105 MSPS.

### PRODUCT HIGHLIGHTS

- **IF Sampling.** The AD6645 maintains outstanding ac performance up to input frequencies of 200 MHz, suitable for multicarrier 3G wideband cellular IF sampling receivers.
- **Pin Compatibility.** The ADC has the same footprint and pin layout as the AD6644 14-bit, 40 MSPS/65 MSPS ADC.
- **SFDR Performance and Oversampling.** Multitone SFDR performance of 100 dBFS can reduce the requirements of high end RF components and allows the use of receive signal processors such as the [AD6620](#), [AD6624/AD6624A](#), or [AD6636](#).

### FUNCTIONAL BLOCK DIAGRAM

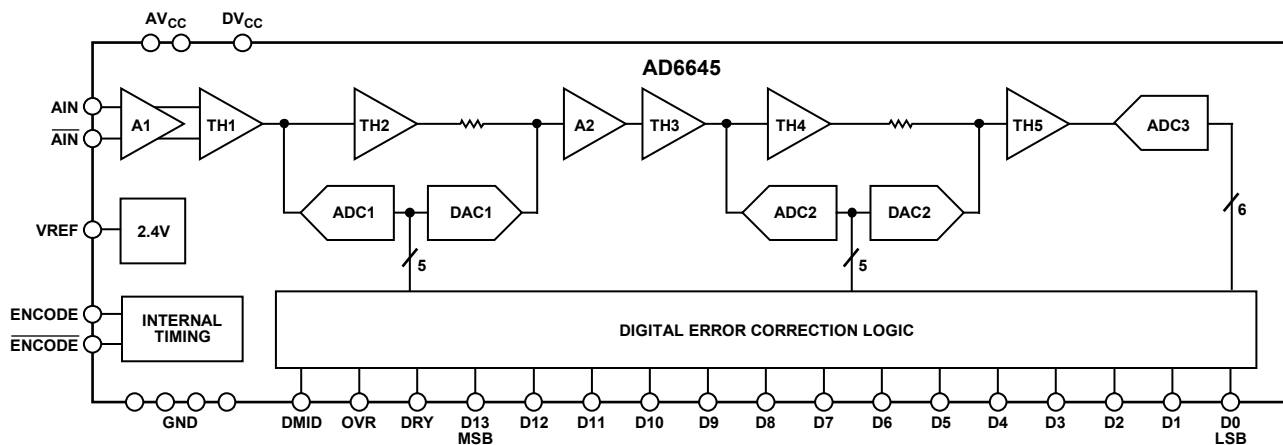


Figure 1.

### Rev. C

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## REVISION HISTORY

### 12/06—Rev. B to Rev. C

Updated Format.....	Universal
Changes to Specifications.....	3
Changes to Jitter Considerations Section.....	19
Changes to Table 8, Bill of Materials.....	20
Changes to Figure 43, Evaluation Board Schematic .....	21
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Updated Outline Dimensions .....	23
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### 7/03—Rev. A to Rev. B.

Changes to Title .....	1
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Changes to Product Description .....	1
Changes to Specifications .....	3
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### 6/02—Rev. 0 to Rev. A.

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## SPECIFICATIONS

### DC SPECIFICATIONS

$AV_{CC} = 5\text{ V}$ ,  $DV_{CC} = 3.3\text{ V}$ ;  $T_{MIN}$  and  $T_{MAX}$  at rated speed grade, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	AD6645ASQ-80			AD6645ASQ-105			Unit
			Min	Typ	Max	Min	Typ	Max	
RESOLUTION			14			14			Bits
ACCURACY			Guaranteed			Guaranteed			
No Missing Codes	Full	II	Guaranteed			Guaranteed			
Offset Error	Full	II	-10	+1.2	+10	-10	+1.2	+10	mV
Gain Error	Full	II	-10	0	+10	-10	0	+10	% FS
Differential Nonlinearity (DNL)	Full	II	-1.0	± 0.25	+1.5	-1.0	± 0.5	+1.5	LSB
Integral Nonlinearity (INL)	Full	V		± 0.5			± 1.5		LSB
TEMPERATURE DRIFT									
Offset Error	Full	V	1.5			1.5			ppm/°C
Gain Error	Full	V	48			48			ppm/°C
POWER SUPPLY REJECTION (PSRR)	25°C	V	± 1.0			± 1.0			mV/V
REFERENCE OUT (VREF) <sup>1</sup>	Full	V	2.4			2.4			V
ANALOG INPUTS (AIN, AIN)									
Differential Input Voltage Range	Full	V	2.2			2.2			V p-p
Differential Input Resistance	Full	V	1			1			kΩ
Differential Input Capacitance	25°C		1.5			1.5			pF
POWER SUPPLY									
Supply Voltages									
$AV_{CC}$	Full	II	4.75	5.0	5.25	4.75	5.0	5.25	V
$DV_{CC}$	Full	II	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Current									
$I_{AV_{CC}}$ ( $AV_{CC} = 5.0\text{ V}$ )	Full	II	275		320	275		320	mA
$I_{DV_{CC}}$ ( $DV_{CC} = 3.3\text{ V}$ )	Full	II	32		45	32		45	mA
Rise Time <sup>2</sup>									
$AV_{CC}$	Full	IV			250	5.0		250	ms
POWER CONSUMPTION	Full	II	1.5		1.75	1.5		1.75	W

<sup>1</sup> VREF is provided for setting the common-mode offset of a differential amplifier such as the AD8138 when a dc-coupled analog input is required. VREF should be buffered if used to drive additional circuit functions.

<sup>2</sup> Specified for dc supplies with linear rise time characteristics.

# AD6645

## DIGITAL SPECIFICATIONS

$AV_{CC} = 5\text{ V}$ ,  $DV_{CC} = 3.3\text{ V}$ ;  $T_{MIN}$  and  $T_{MAX}$  at rated speed grade, unless otherwise noted.

Table 2.

Parameter (Conditions)	Temp	Test Level	AD6645ASQ-80			AD6645ASQ-105			Unit
			Min	Typ	Max	Min	Typ	Max	
ENCODE INPUTS (ENC, $\overline{\text{ENC}}$ )									
Differential Input Voltage <sup>1</sup>	Full	IV	0.4			0.4			V p-p
Differential Input Resistance	25°C	V		10			10		k $\Omega$
Differential Input Capacitance	25°C	V		2.5			2.5		pF
LOGIC OUTPUTS (D13 to D0, DRY, OVR)									
Logic Compatibility				CMOS			CMOS		
Logic 1 Voltage ( $DV_{CC} = 3.3\text{ V}$ ) <sup>2</sup>	Full	II	2.85	$DV_{CC} - 2$		2.85	$DV_{CC} - 2$		V
Logic 0 Voltage ( $DV_{CC} = 3.3\text{ V}$ ) <sup>2</sup>	Full	II		0.2	0.5		0.2	0.5	V
Output Coding				Twos complement			Twos complement		
DMID	Full	V		$DV_{CC}/2$			$DV_{CC}/2$		V

<sup>1</sup> All ac specifications tested by driving ENCODE and  $\overline{\text{ENC}}$  differentially.

<sup>2</sup> Digital output logic levels:  $DV_{CC} = 3.3\text{ V}$ ,  $C_{LOAD} = 10\text{ pF}$ . Capacitive loads  $>10\text{ pF}$  degrades performance.

## AC SPECIFICATIONS

All ac specifications tested by driving ENCODE and  $\overline{\text{ENC}}$  differentially.

$AV_{CC} = 5\text{ V}$ ,  $DV_{CC} = 3.3\text{ V}$ ; ENCODE,  $\overline{\text{ENC}}$ ,  $T_{MIN}$  and  $T_{MAX}$  at rated speed grade, unless otherwise noted.

Table 3.

Parameter	Temp	Test Level	AD6645ASQ-80			AD6645ASQ-105			Unit	Conditions
			Min	Typ	Max	Min	Typ	Max		
SNR										
Analog Input @ -1 dBFS	25°C	V		75.0			75.0		dB	@ 15.5 MHz
	Full	II	72.5	74.5					dB	@ 30.5 MHz
	25°C	I				72.5	74.5		dB	@ 37.7 MHz
	Full	II	72.0	73.5		72.0	73.5		dB	@ 70.0 MHz
	25°C	V		73.0			73.0		dB	@ 150.0 MHz
	25°C	V		72.0			72.0		dB	@ 200.0 MHz
SINAD										
Analog Input @ -1 dBFS	25°C	V		75.0			75.0		dB	@ 15.5 MHz
	Full	II	72.5	74.5					dB	@ 30.5 MHz
	25°C	I				72.5	74.5		dB	@ 37.7 MHz
	Full	V		73.0			73.0		dB	@ 70.0 MHz
	25°C	V		68.5			67.5		dB	@ 150.0 MHz
	25°C	V		62.5			62.5		dB	@ 200.0 MHz
WORST HARMONIC (Second or Third)										
Analog Input @ -1 dBFS	25°C	V		93.0			93.1		dBc	@ 15.5 MHz
	Full	II	85.0	93.0					dBc	@ 30.5 MHz
	25°C	I				85.0	93.0		dBc	@ 37.7 MHz
	Full	V		89.0			87.0		dBc	@ 70.0 MHz
	25°C	V		70.0			70.0		dBc	@ 150.0 MHz
	25°C	V		63.5			63.5		dBc	@ 200.0 MHz

Parameter	Temp	Test Level	AD6645ASQ-80			AD6645ASQ-105			Unit	Conditions
			Min	Typ	Max	Min	Typ	Max		
WORST HARMONIC (Fourth or Higher) Analog Input @ -1 dBFS	25°C	V		96.0			96.0		dBc	@ 15.5 MHz
	Full	II	85.0	95.0						@ 30.5 MHz
	25°C	I				86.0	95.0			@ 37.7 MHz
	Full	V		90.0			90.0			@ 70.0 MHz
	25°C	V		90.0			90.0			@ 150.0 MHz
	25°C	V		88.0			88.0			@ 200.0 MHz
TWO-TONE SFDR	25°C	V		100			98.0		dBFS	@ 30.5 MHz <sup>1,2</sup>
	25°C	V		100			98.0			@ 55.0 MHz <sup>1,3</sup>
	25°C	V					98.0			@ 70.0 MHz <sup>1,4</sup>
TWO-TONE IMD REJECTION <sup>2,3</sup> F1, F2 @ -7 dBFS	25°C	V		90			90		dBc	
ANALOG INPUT BANDWIDTH	25°C	V		270			270		MHz	

<sup>1</sup> Analog input signal power swept from -10 dBFS to -100 dBFS.

<sup>2</sup> F1 = 30.5 MHz, F2 = 31.5 MHz.

<sup>3</sup> F1 = 55.25 MHz, F2 = 56.25 MHz.

<sup>4</sup> F1 = 69.1 MHz, F2 = 71.1 MHz.

## SWITCHING SPECIFICATIONS

AV<sub>CC</sub> = 5 V, DV<sub>CC</sub> = 3.3 V; ENCODE,  $\overline{\text{ENCODE}}$ , T<sub>MIN</sub> and T<sub>MAX</sub> at rated speed grade, unless otherwise noted.

Table 4.

Parameter	Symbol	Temp	Test Level	AD6645ASQ-80			AD6645ASQ-105			Unit
				Min	Typ	Max	Min	Typ	Max	
Maximum Conversion Rate		Full	II	80			105			MSPS
Minimum Conversion Rate		Full	IV			30			30	MSPS
ENCODE Pulse Width High, (t <sub>ENCH</sub> ) <sup>1</sup>		Full	IV	5.625			4.286			ns
ENCODE Pulse Width Low, (t <sub>ENCL</sub> ) <sup>1</sup>		Full	IV	5.625			4.286			ns
ENCODE Input Parameters <sup>2</sup>										
Encode Period <sup>2</sup>	t <sub>ENC</sub>	Full	V		12.5			9.5		ns
Encode Pulse Width High <sup>2</sup>	t <sub>ENCH</sub>	Full	V		6.25			4.75		ns
Encode Pulse Width Low	t <sub>ENCL</sub>	Full	V		6.25			4.75		ns
ENCODE/DataReady										
Encode Rising to DataReady Falling	t <sub>DR</sub>	Full	V	1.0	2.0	3.1	1.0	2.0	3.1	ns
Encode Rising to DataReady Rising (50% Duty Cycle)	t <sub>E_DR</sub>	Full	V		t <sub>ENCH</sub> + t <sub>DR</sub>			t <sub>ENCH</sub> + t <sub>DR</sub>		ns
		Full	V	7.3	8.3	9.4	5.7	6.75	7.9	ns
ENCODE/DATA (D13:0), OVR										
ENC to DATA Falling Low	t <sub>E_FL</sub>	Full	V	2.4	4.7	7.0	2.4	4.7	7.0	ns
ENC to DATA Rising Low <sup>3</sup>	t <sub>E_RL</sub>	Full	V	1.4	3.0	4.7	1.4	3.0	4.7	ns
ENCODE to DATA Delay <sup>3</sup> (Hold Time)	t <sub>H_E</sub>	Full	V	1.4	3.0	4.7	1.4	3.0	4.7	ns
ENCODE to DATA Delay (Setup Time)	t <sub>S_E</sub>	Full	V	t <sub>ENC-</sub> t <sub>E_FL(max)</sub>			t <sub>ENC-</sub> t <sub>E_FL(max)</sub>			ns
					t <sub>ENC-</sub> t <sub>E_FL(typ)</sub>			t <sub>ENC-</sub> t <sub>E_FL(typ)</sub>		ns
						t <sub>ENC-</sub> t <sub>E_FL(min)</sub>			t <sub>ENC-</sub> t <sub>E_FL(min)</sub>	ns
(50% Duty Cycle)		Full	V	5.3	7.6	10.0	2.3	4.8	7.0	ns

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Parameter	Symbol	Temp	Test Level	AD6645ASQ-80			AD6645ASQ-105			Unit
				Min	Typ	Max	Min	Typ	Max	
DataReady (DRY <sup>4</sup> )/DATA, OVR										
DataReady to DATA Delay (Hold Time) (50% Duty Cycle)	$t_{H\_DR}$	Full	V		Note 5		Note 5			ns
DataReady to DATA Delay (Setup Time) (50% Duty Cycle)	$t_{S\_DR}$	Full	V	6.6	7.2	7.9	5.1	5.7	6.4	ns
APERTURE DELAY	$t_A$	25°C	V		-500			-500		ps
APERTURE UNCERTAINTY (Jitter)	$t_j$	25°C	V		0.1		0.1			ps rms

<sup>1</sup> Several timing parameters are a function of  $t_{ENCL}$  and  $t_{ENCH}$ .

<sup>2</sup> Several timing parameters are a function of  $t_{ENC}$  and  $t_{ENCH}$ .

<sup>3</sup> ENCODE TO DATA Delay (Hold Time) is the absolute minimum propagation delay through the analog-to-digital converter,  $t_{E\_RL} = t_{H\_E}$ .

<sup>4</sup> DRY is an inverted and delayed version of the encode clock. Any change in the duty cycle of the clock will correspondingly change the duty cycle of DRY.

<sup>5</sup> DataReady to DATA Delay ( $t_{H\_DR}$  and  $t_{S\_DR}$ ) is calculated relative to rated speed grade and is dependent on  $t_{ENC}$  and duty cycle.

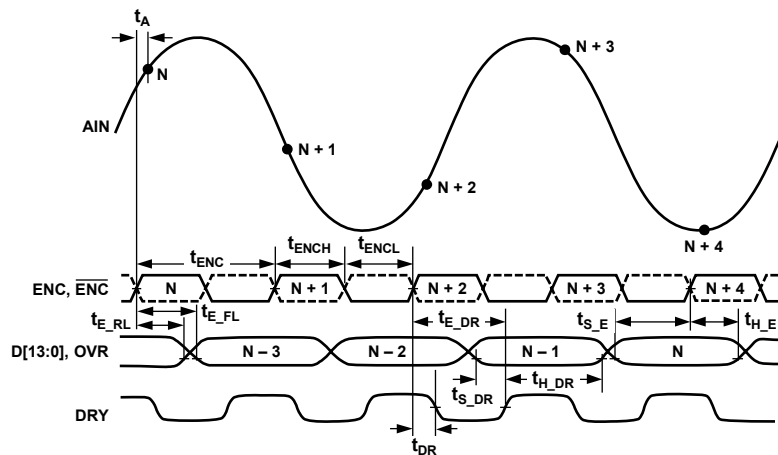


Figure 2. Timing Diagram

02647-002

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Electrical	
$AV_{CC}$ Voltage	0 V to 7 V
$DV_{CC}$ Voltage	0 V to 7 V
Analog Input Voltage	0 V to $AV_{CC}$
Analog Input Current	25 mA
Digital Input Voltage	0 V to $AV_{CC}$
Digital Output Current	4 mA
Environmental	
–80 Operating Temperature Range (Ambient)	–40°C to +85°C
–105 Operating Temperature Range (Ambient)	–10°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	–65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL CHARACTERISTICS

52-lead PowerQuad 4 (LQFP\_PQ4)

$\theta_{JA} = 23^{\circ}\text{C}/\text{W}$  soldered slug, no airflow

$\theta_{JA} = 17^{\circ}\text{C}/\text{W}$  soldered slug, 200 LFPM airflow

$\theta_{JA} = 30^{\circ}\text{C}/\text{W}$  unsoldered slug, no airflow

$\theta_{JA} = 24^{\circ}\text{C}/\text{W}$  unsoldered slug, 200 LFPM airflow

$\theta_{JC} = 2^{\circ}\text{C}/\text{W}$  bottom of package (heatslug)

Typical 4-layer JEDEC board horizontal orientation

## EXPLANATION OF TEST LEVELS

Test Level

- I. 100% production tested.
- II. 100% production tested at 25°C and guaranteed by design and characterization at temperature extremes.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# AD6645

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

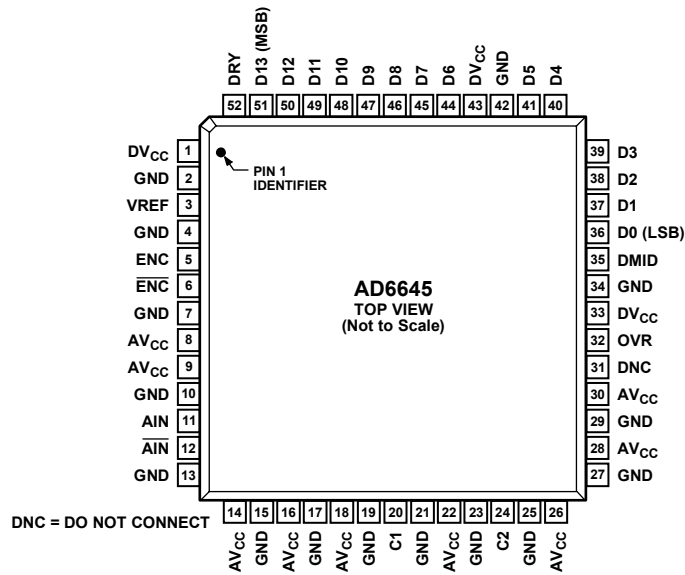


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 33, 43	DV <sub>CC</sub>	3.3 V Power Supply (Digital) Output Stage Only.
2, 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, 29, 34, 42	GND	Ground.
3	VREF	2.4 V Reference. Bypass to ground with a 0.1 μF microwave chip capacitor.
5	ENC	Encode Input. Conversion initiated on rising edge.
6	$\overline{\text{ENC}}$	Complement of ENC, Differential Input.
8, 9, 14, 16, 18, 22, 26, 28, 30	AV <sub>CC</sub>	5 V Analog Power Supply.
11	A $\overline{\text{IN}}$	Analog Input.
12	A $\overline{\text{IN}}$	Complement of A $\overline{\text{IN}}$ , Differential Analog Input.
20	C1	Internal Voltage Reference. Bypass to ground with a 0.1 μF chip capacitor.
24	C2	Internal Voltage Reference. Bypass to ground with a 0.1 μF chip capacitor.
31	DNC	Do not connect this pin.
32	OVR	Overrange Bit. A logic level high indicates analog input exceeds ±FS.
35	DMID	Output Data Voltage Midpoint. Approximately equal to (DV <sub>CC</sub> )/2.
36	D0 (LSB)	Digital Output Bit (Least Significant Bit); Twos Complement.
37 to 41, 44 to 50	D1 to D5, D6 to D12	Digital Output Bits in Twos Complement.
51	D13 (MSB)	Digital Output Bit (Most Significant Bit); Twos Complement.
52	DRY	DataReady Output.



## TERMINOLOGY

### Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

### Aperture Delay

The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

### Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

### Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance

The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

### Differential Analog Input Voltage Range

The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the inputs' phase 180 degrees and taking the peak measurement again. Then the difference is computed between both peak measurements.

### Differential Nonlinearity

The deviation of any code width from an ideal 1 LSB step.

### Encode Pulse Width/Duty Cycle

Pulse width high is the minimum amount of time that the ENCODE pulse should be left in Logic 1 state to achieve rated performance; pulse width low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing  $t_{ENCH}$  in Table 4. At a given clock rate, these specifications define an acceptable ENCODE duty cycle.

### Full-Scale Input Power

Expressed in dBm. Computed using the following equation:

$$Power_{Full-Scale} = 10 \log \left[ \frac{V^2_{Full-Scale\ rms}}{|Z|_{Input} \cdot 0.001} \right]$$

### Harmonic Distortion, Second

The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

### Harmonic Distortion, Third

The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

### Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least square curve fit.

### Minimum Conversion Rate

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

### Maximum Conversion Rate

The encode rate at which parametric testing is performed.

### Noise (For Any Range Within the ADC)

$$V_{NOISE} = \sqrt{|Z| \times 0.001 \times 10 \left( \frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10} \right)}$$

where:

Z is the input impedance.

FS is the full scale of the device for the frequency in question.

SNR is the value for the particular input level.

Signal is the signal level within the ADC reported in dB below full scale. This value includes both thermal noise and quantization noise.

### Output Propagation Delay

The delay between a differential crossing of ENCODE and ENCODE and the time when all output data bits are within valid logic levels.

### Power Supply Rejection Ratio (PSSR)

The ratio of a change in input offset voltage to a change in power supply voltage.

### Power Supply Rise Time

The time from when the dc supply is initiated until the supply output reaches the minimum specified operating voltage for the ADC. The dc level is measured at the supply pin(s) of the ADC.

### Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

### Signal-to-Noise Ratio (Without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

# AD6645

## **Spurious-Free Dynamic Range (SFDR)**

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (that is, degrades as signal level is lowered) or dBFS (always related back to converter full scale).

## **Two-Tone Intermodulation Distortion Rejection**

The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product, reported in dBc.

## **Two-Tone SFDR**

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product, may be reported in dBc (that is, degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

## **Worst Other Spur**

The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonics), reported in dBc.

# EQUIVALENT CIRCUITS

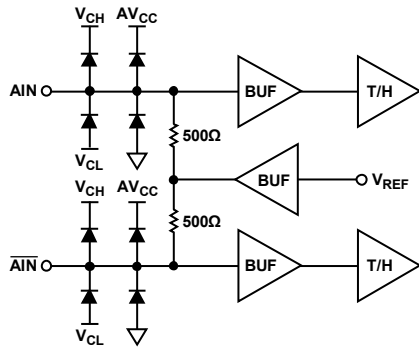


Figure 4. Analog Input Stage

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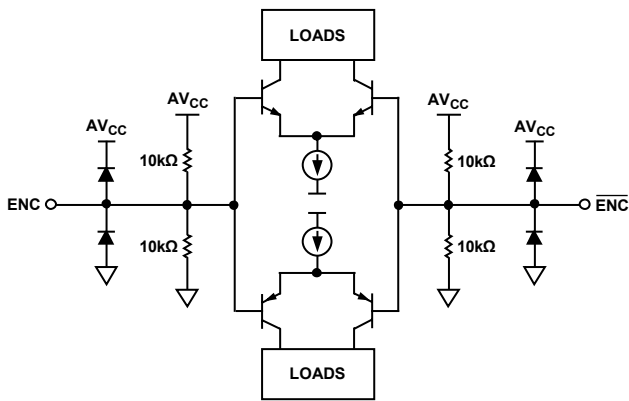


Figure 5. Encode Inputs

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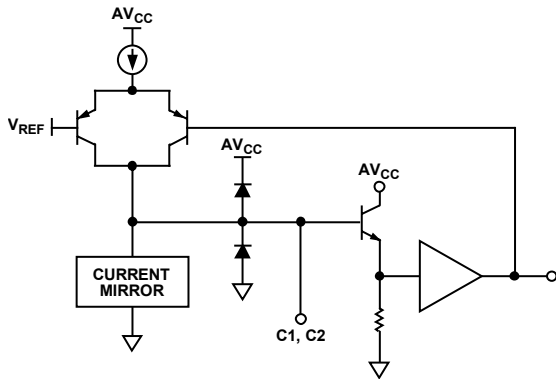


Figure 6. Compensation Pin, C1 or C2

02847-006

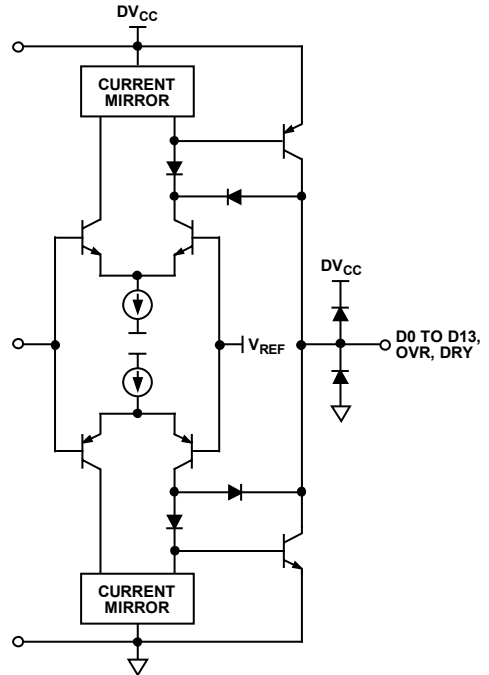


Figure 7. Digital Output Stage

02847-007

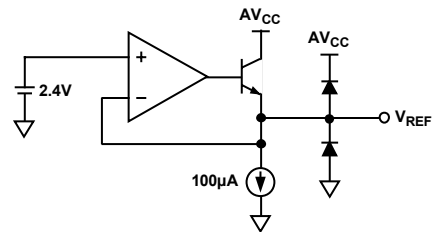


Figure 8. 2.4 V Reference

02847-008

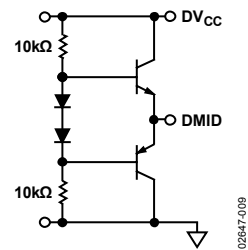


Figure 9. DMID Reference

02847-009

TYPICAL PERFORMANCE CHARACTERISTICS

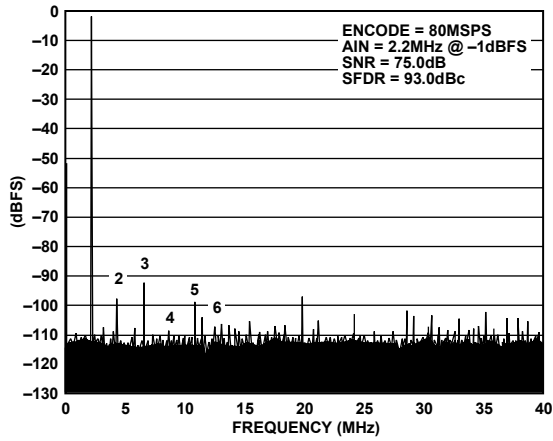


Figure 10. Single Tone @ 2.2 MHz

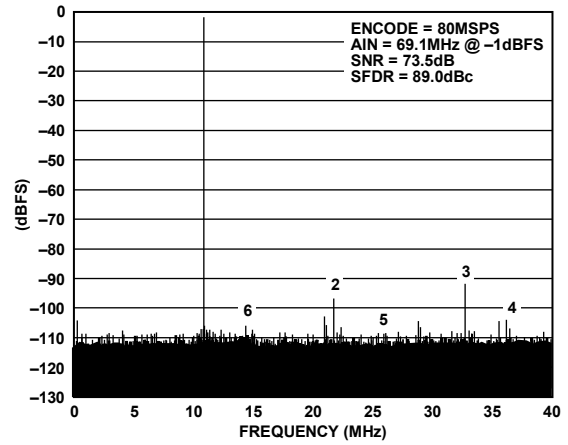


Figure 13. Single Tone @ 69.1 MHz

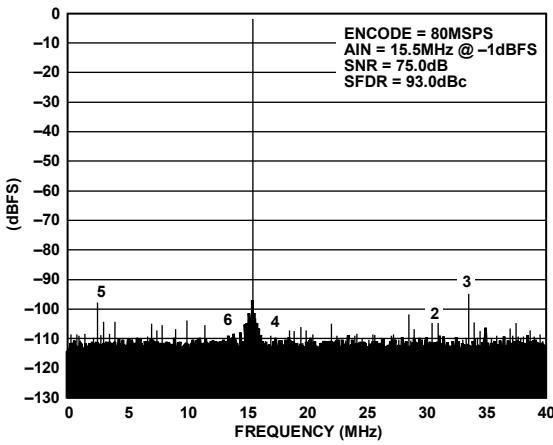


Figure 11. Single Tone @ 15.5 MHz

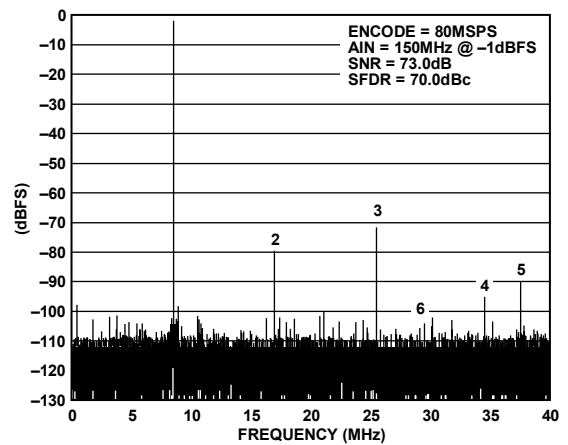


Figure 14. Single Tone @ 150 MHz

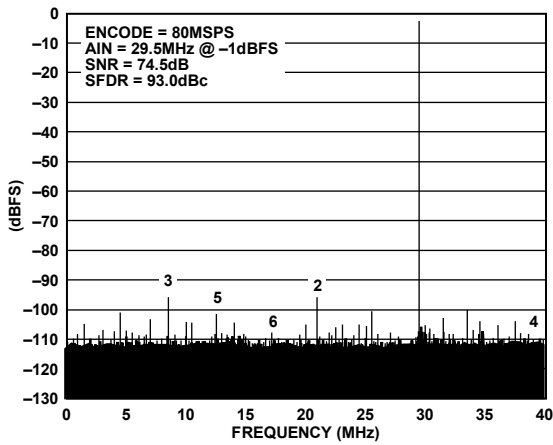


Figure 12. Single Tone @ 29.5 MHz

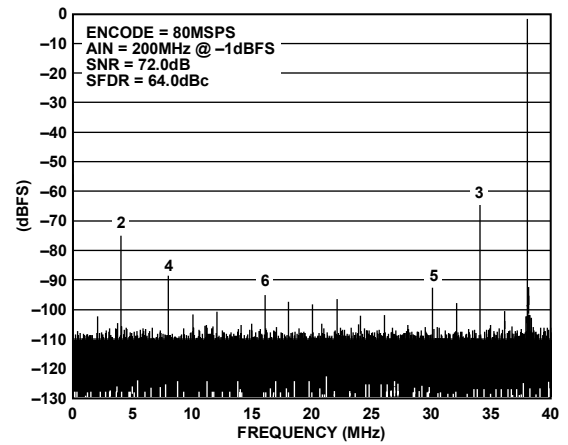


Figure 15. Single Tone @ 200 MHz

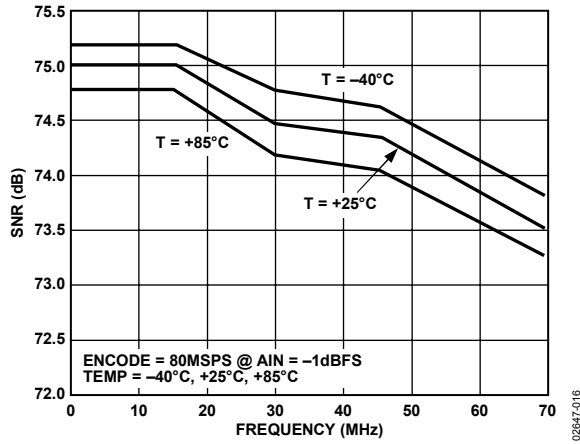


Figure 16. Noise vs. Analog Frequency

02647-016

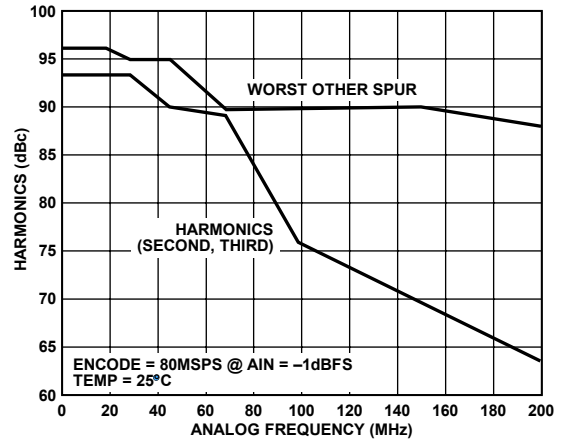


Figure 19. Harmonics vs. Analog Frequency (IF)

02647-019

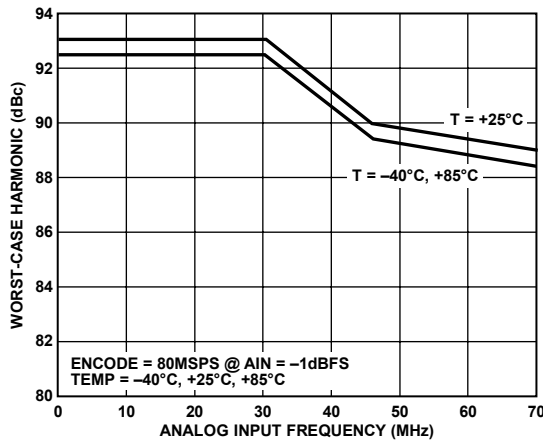


Figure 17. Worst-Case Harmonics vs. Analog Frequency

02647-017

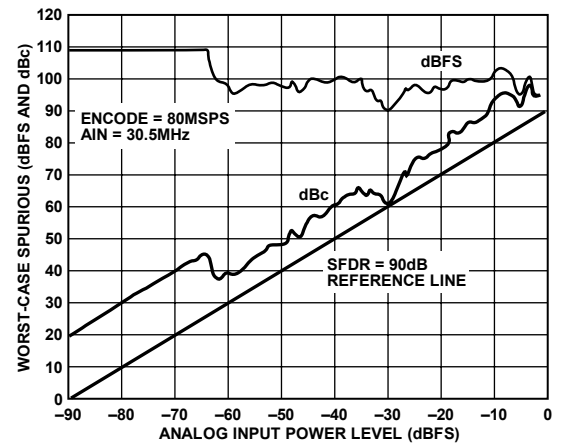


Figure 20. Single-Tone SFDR @ 30.5 MHz

02647-020

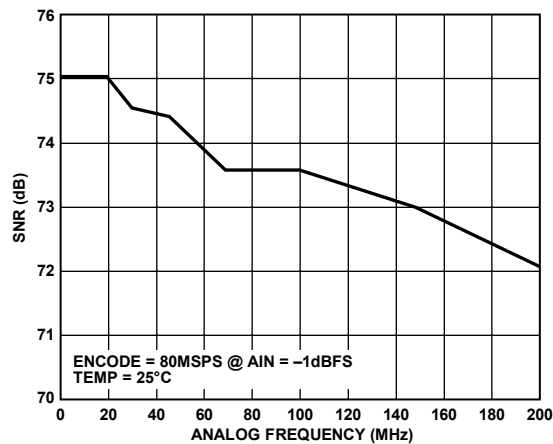


Figure 18. Noise vs. Analog Frequency (IF)

02647-018

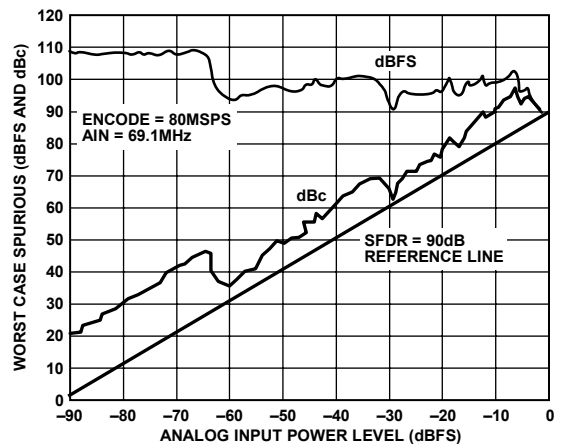


Figure 21. Single-Tone SFDR @ 69.1 MHz

02647-021

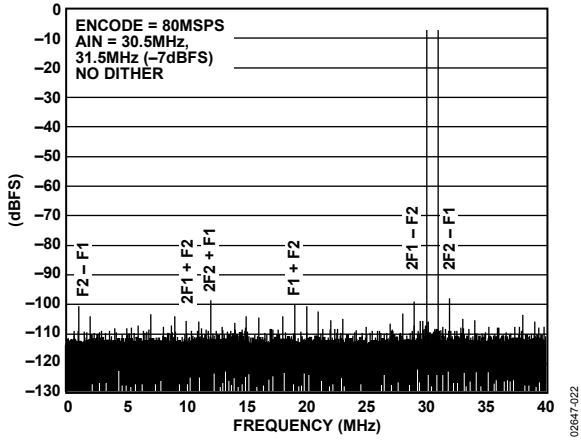


Figure 22. Two-Tone SFDR @ 30.5 MHz and 31.5 MHz

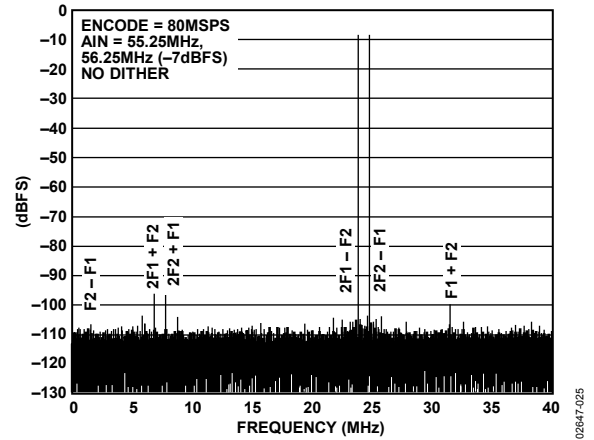


Figure 25. Two-Tone SFDR @ 55.25 MHz and 56.25 MHz

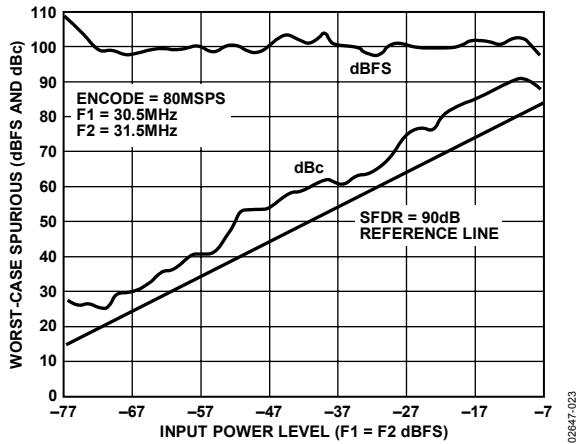


Figure 23. Two-Tone SFDR @ 30.5 MHz and 31.5 MHz

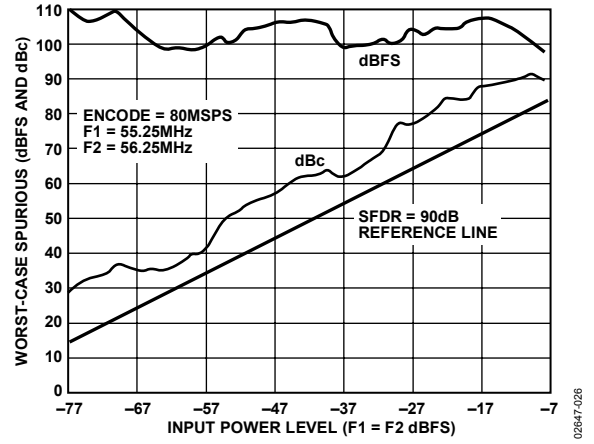


Figure 26. Two-Tone SFDR @ 55.25 MHz and 56.25 MHz

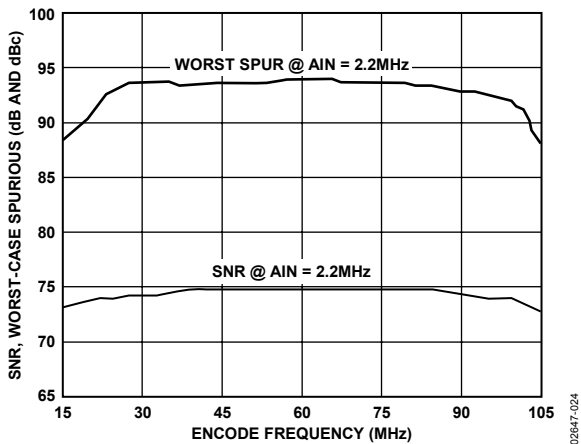


Figure 24. SNR, Worst Spurious vs. Encode @ 2.2 MHz

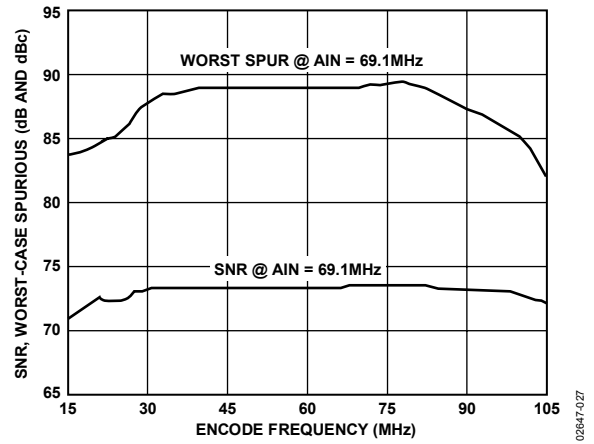


Figure 27. SNR, Worst Spurious vs. Encode @ 69.1 MHz

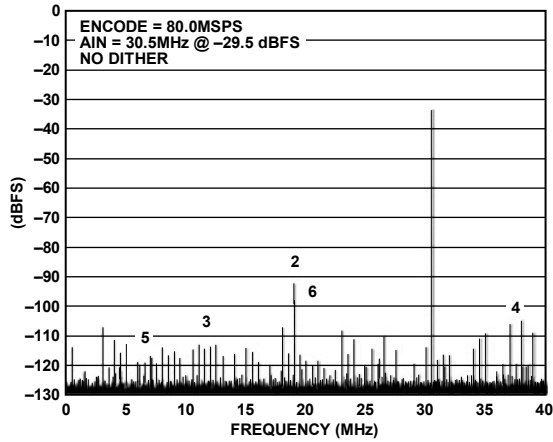


Figure 28. 1 Meg FFT Without Dither

02847-028

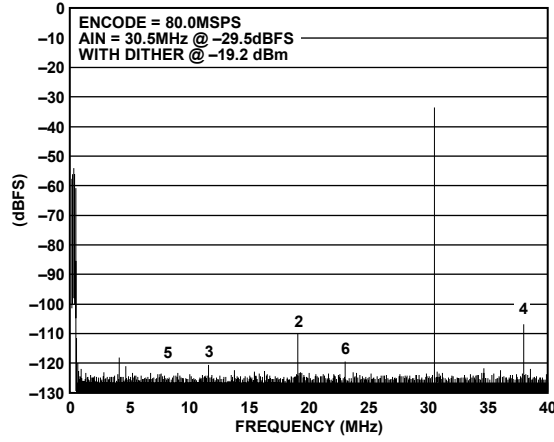


Figure 31. 1 Meg FFT with Dither

02847-031

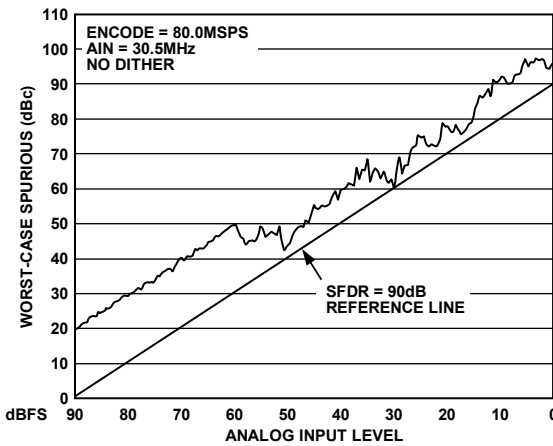


Figure 29. SFDR Without Dither

02847-029

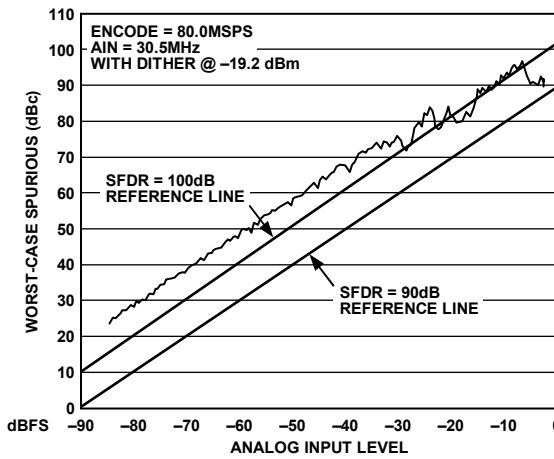


Figure 32. SFDR with Dither

02847-032

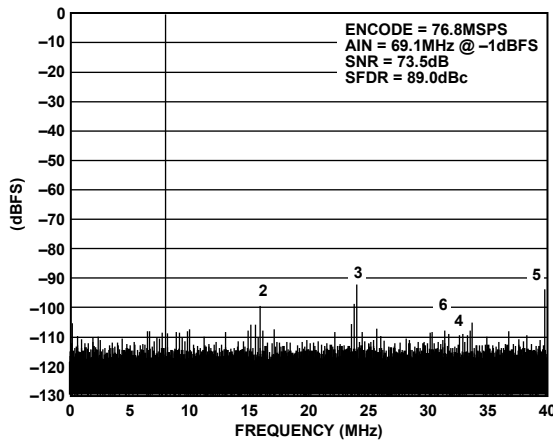


Figure 30. Single Tone @ 69.1 MHz, Encode = 76.8 MSPS

02847-030

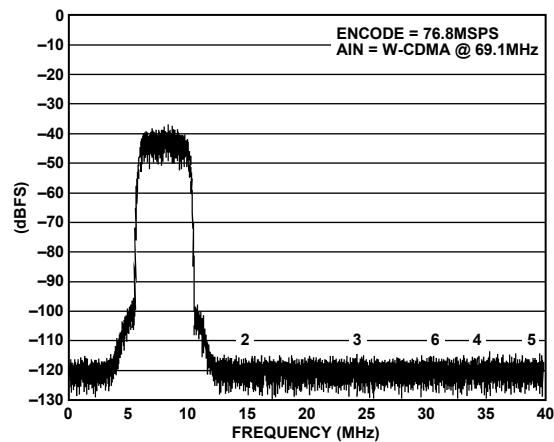


Figure 33. W-CDMA Tone @ 69.1 MHz, Encode = 76.8 MSPS

02847-033

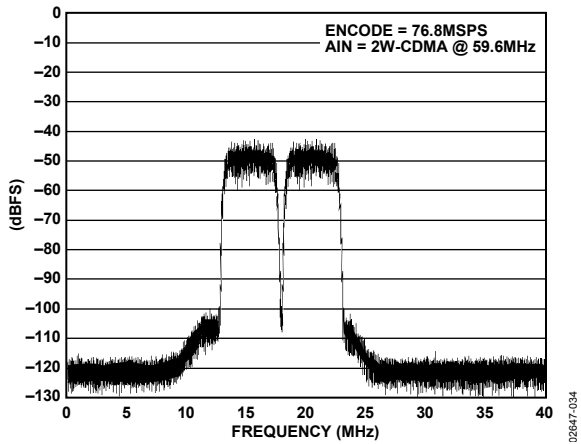


Figure 34. 2 W-CDMA Carriers @ AIN = 59.6 MHz, Encode = 76.8 MS/SPS

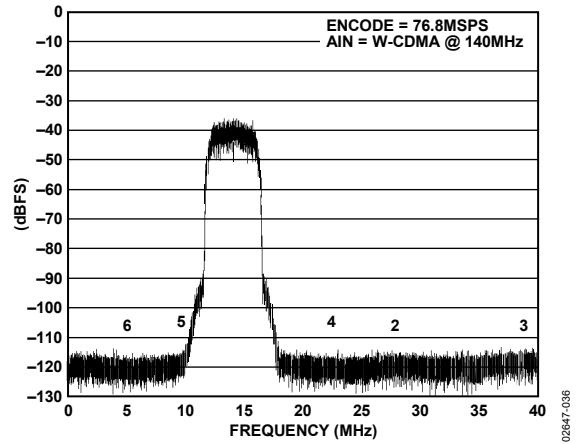


Figure 36. W-CDMA Tone @ 140 MHz, Encode = 76.8 MS/SPS

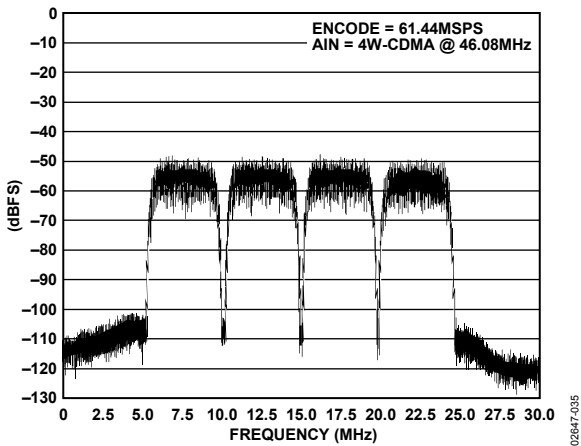


Figure 35. 4 W-CDMA Carriers @ AIN = 46.08 MHz, Encode = 61.44 MS/SPS

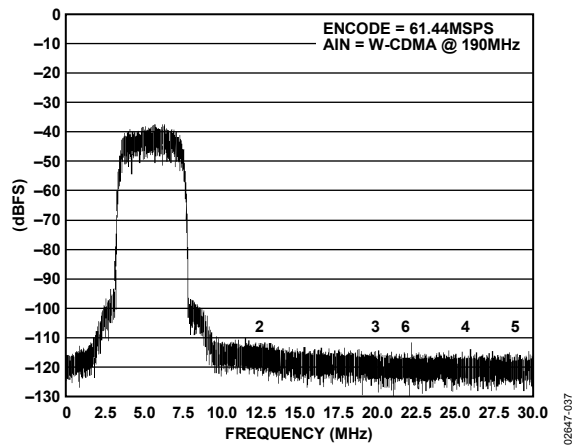


Figure 37. W-CDMA Tone @ 190 MHz, Encode = 61.44 MS/SPS



## THEORY OF OPERATION

The AD6645 analog-to-digital converter (ADC) employs a 3-stage subrange architecture. This design approach achieves the required accuracy and speed while maintaining low power and small die size.

As shown in the Functional Block Diagram, the AD6645 has complementary analog input pins, AIN and  $\overline{\text{AIN}}$ . Each analog input is centered at 2.4 V and should swing  $\pm 0.55$  V around this reference (see Figure 4). Since AIN and  $\overline{\text{AIN}}$  are 180 degrees out of phase, the differential analog input signal is 2.2 V p-p.

Both analog inputs are buffered prior to the first track-and-hold, TH1. The high state of the ENCODE pulse places TH1 in hold mode. The held value of TH1 is applied to the input of a 5-bit coarse ADC1. The digital output of ADC1 drives a 5-bit digital-to-analog converter, DAC1. DAC1 requires 14 bits of precision that is achieved through laser trimming. The output of DAC1 is subtracted from the delayed analog signal at the input of TH3 to generate a first residue signal. TH2 provides an analog pipeline delay to compensate for the digital delay of ADC1.

The first residue signal is applied to a second conversion stage consisting of a 5-bit ADC2, a 5-bit DAC2, and a pipeline TH4. The second DAC requires 10 bits of precision, which is met by the process with no trim. The input to TH5 is a second residue signal generated by subtracting the quantized output of DAC2 from the first residue signal held by TH4. TH5 drives a final 6-bit ADC3.

The digital outputs from ADC1, ADC2, and ADC3 are added together and corrected in the digital error correction logic to generate the final output data. The result is a 14-bit parallel digital CMOS-compatible word, coded as twos complement.

### APPLYING THE AD6645

#### Encoding the AD6645

The AD6645 encode signal must be a high quality, extremely low phase noise source to prevent degradation of performance. Maintaining 14-bit accuracy places a premium on encode clock phase noise. SNR performance can easily degrade by 3 dB to 4 dB with 70 MHz analog input signals when using a high jitter clock source. See [AN-501](#), *Aperture Uncertainty and ADC System Performance* for complete details.

For optimum performance, the AD6645 must be clocked differentially. The encode signal is usually ac-coupled into the ENC and  $\overline{\text{ENC}}$  pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 38 shows one preferred method for clocking the AD6645. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limits excessive amplitude swings from the clock into the AD6645 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other

portions of the AD6645, and limits the noise presented to the encode inputs.

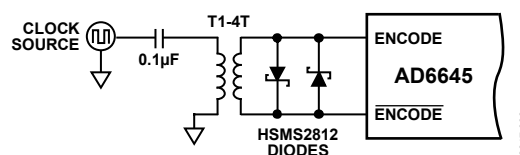


Figure 38. Crystal Clock Oscillator, Differential Encode

If a low jitter clock is available, another option is to ac-couple a differential ECL/PECL signal to the encode input pins as shown in Figure 39. The MC100EL16 (or same family) from ON-SEMI offers excellent jitter performance.

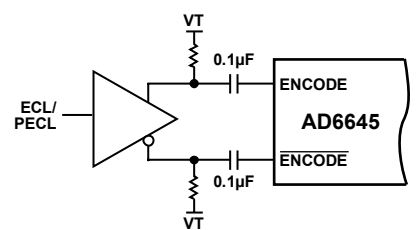


Figure 39. Differential ECL for Encode

#### Driving the Analog Inputs

As with most new high speed, high dynamic range analog-to-digital converters, the analog input to the AD6645 is differential. Differential inputs improve on-chip performance as signals are processed through attenuation and gain stages. Most of the improvement is a result of differential analog stages having high rejection of even-order harmonics. There are also benefits at the PCB level. First, differential inputs have high common-mode rejection of stray signals such as ground and power noise. Second, they provide good rejection of common-mode signals such as local oscillator feedthrough.

The AD6645 analog input voltage range is offset from ground by 2.4 V. Each analog input connects through a 500  $\Omega$  resistor to the 2.4 V bias voltage and to the input of a differential buffer (see Figure 4). The resistor network on the input properly biases the followers for maximum linearity and range. Therefore, the analog source driving the AD6645 should be ac-coupled to the input pins. Since the differential input impedance of the AD6645 is 1 k $\Omega$ , the analog input power requirement is only  $-2$  dBm, simplifying the driver amplifier in many cases. To take full advantage of this high input impedance, a 20:1 RF transformer is required. This is a large ratio and could result in unsatisfactory performance. In this case, a lower step-up ratio can be used. The recommended method for driving the analog input of the AD6645 is to use a 4:1 RF transformer. For example, if  $R_T$  is set to 60.4  $\Omega$  and  $R_S$  is set to 25  $\Omega$ , along with a 4:1 impedance ratio transformer, the input would match to a 50  $\Omega$  source with a full-scale drive of 4.8 dBm. Series resistors ( $R_S$ ) on the secondary side of the transformer should be used to isolate the transformer from the A/D. This limits the amount of

# AD6645

dynamic current from the A/D flowing back into the secondary of the transformer. The 50  $\Omega$  impedance matching can also be incorporated on the secondary side of the transformer as shown in the evaluation board schematic (see Figure 43).

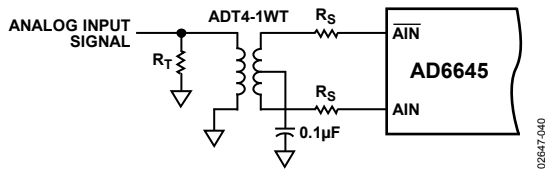


Figure 40. Transformer-Coupled Analog Input Circuit

In applications where dc-coupling is required, a differential output op amp such as the AD8138 from Analog Devices can be used to drive the AD6645 (see Figure 41). The AD8138 op amp provides single-ended-to-differential conversion, which reduces overall system cost and minimizes layout requirements.

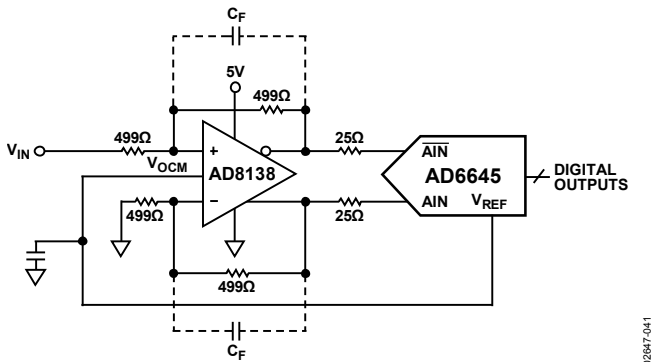


Figure 41. DC-Coupled Analog Input Circuit

## Power Supplies

Care should be taken when selecting a power source. The use of linear dc supplies with rise times of <math><45\text{ ms}</math> is highly recommended. Switching supplies tend to have radiated components that may be received by the AD6645. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1  $\mu\text{F}$  chip capacitors.

The AD6645 has separate digital and analog power supply pins. The analog supplies are denoted as  $AV_{CC}$  and the digital supply pins are denoted as  $DV_{CC}$ . Although analog and digital supplies can be tied together, best performance is achieved when the supplies are separate because the fast digital output swings can couple switching currents back into the analog supplies. Note that  $AV_{CC}$  must be held within 5% of 5 V. The AD6645 is specified for  $DV_{CC} = 3.3\text{ V}$ , a common supply for digital ASICs.

## Digital Outputs

Care must be taken when designing the data receivers for the AD6645. It is recommended that the digital outputs drive a series resistor followed by a gate such as the 74LCX574. To minimize capacitive loading, there should only be one gate on each output pin. An example of this is shown in the evaluation

board schematic of Figure 43. The digital outputs of the AD6645 have a constant output slew rate of 1 V/ns. A typical CMOS gate combined with a PCB trace have a load of approximately 10 pF. Therefore, as each bit switches, 10 mA ( $10\text{ pF} \times 1\text{ V} \div 1\text{ ns}$ ) of dynamic current per bit flow in or out of the device. A full-scale transition can cause up to 140 mA ( $14\text{ bits} \times 10\text{ mA/bit}$ ) of current to flow through the output stages. The series resistors should be placed as close to the AD6645 as possible to limit the amount of current that can flow into the output stage. These switching currents are confined between ground and the  $DV_{CC}$  pin. Standard TTL gates should be avoided since they can appreciably add to the dynamic switching currents of the AD6645. It should be noted that extra capacitive loading increases output timing and invalidates timing specifications. Digital output timing is guaranteed for output loads up to 10 pF. Digital output states for given analog input levels are shown in Table 7.

## Grounding

For optimum performance, it is highly recommended that a common ground be utilized between the analog and digital power planes. The primary concern with splitting grounds is that dynamic currents may be forced to travel significant distances in the system before recombining back at the common source ground. This can result in a large, undesirable ground loop. The most common place for this to occur is on the digital outputs of the ADC. Ground loops can contribute to digital noise being coupled back onto the ADC front end. This can manifest itself as either harmonic spurs, or very high order spurious products that can cause excessive spikes on the noise floor. This noise coupling is less likely to occur at lower clock speeds since the digital noise has more time to settle between samples. In general, splitting the analog and digital grounds can frequently contribute to undesirable EMI-RFI and should therefore be avoided.

Conversely, if not properly implemented, common grounding can actually impose additional noise issues since the digital ground currents are riding on top of the analog ground currents in close proximity to the ADC input. To further minimize the potential for noise coupling, it is highly recommended that multiple ground return traces/vias be placed such that the digital output currents do not flow back towards the analog front end, but are routed quickly away from the ADC. This does not require a split in the ground plane and can be accomplished by simply placing substantial ground connections directly back to the supply at a point between the analog front end and the digital outputs. The judicious use of ceramic chip capacitors between the power supply and ground planes also helps suppress digital noise. The layout should incorporate enough bulk capacitance to supply the peak current requirements during switching periods.

## LAYOUT INFORMATION

The schematic of the evaluation board (see Figure 43) represents a typical implementation of the AD6645. A multilayer board is recommended to achieve best results. It is highly recommended that high quality, ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. The pinout of the AD6645 facilitates ease of use in the implementation of high frequency, high resolution design practices. All of the digital outputs are segregated to two sides of the chip, with the inputs on the opposite side for isolation purposes.

Care should be taken when routing the digital output traces. To prevent coupling through the digital outputs into the analog portion of the AD6645, minimal capacitive loading should be placed on these outputs. It is recommended that a fanout of only one gate should be used for all AD6645 digital outputs.

The layout of the encode circuit is equally critical. Any noise received on this circuitry results in corruption in the digitization process and lower overall performance. The encode clock must be isolated from the digital outputs and the analog inputs.

**Table 7. Twos Complement Output Coding**

AIN Level	AIN Level	Output State	Output Code
$V_{REF} + 0.55 V$	$V_{REF} - 0.55 V$	Positive FS	01 1111 1111 1111
$V_{REF}$	$V_{REF}$	Midscale	00...0/11...1
$V_{REF} - 0.55 V$	$V_{REF} + 0.55 V$	Negative FS	10 0000 0000 0000

### Jitter Considerations

The signal-to-noise ratio (SNR) for an ADC can be predicted. When normalized to ADC codes, the following equation accurately predicts the SNR based on three terms: jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter.

$$SNR = 1.76 - 20 \log \left[ \left( 2\pi \times F_{ANALOG} \times t_{j_{rms}} \right)^2 + \left( \frac{1+\epsilon}{2^n} \right)^2 + \left( \frac{2 \times \sqrt{2} \times V_{NOISE_{rms}}}{2^n} \right)^2 \right]^{1/2}$$

where:

$F_{ANALOG}$  is the analog input frequency.

$t_{j_{rms}}$  is the rms jitter of the encode (rms sum of encode source and internal encode circuitry).

$\epsilon$  is the average DNL of the ADC (typically 0.41 LSB).

$n$  is the number of bits in the ADC.

$V_{NOISE_{rms}}$  is the voltage rms thermal noise that refers to the analog input of the ADC (typically 0.9 LSB rms).

For a 14-bit analog-to-digital converter, like the AD6645, aperture jitter can greatly affect the SNR performance as the analog frequency is increased. Figure 42 shows a family of curves that demonstrate the expected SNR performance of the AD6645 as jitter increases. The chart is derived from the preceding equation.

For a complete discussion of aperture jitter, see [AN-756](#), *Sampled Systems and the Effects of Clock Phase Noise and Jitter*. The [AN-756](#) application note can be found on [www.analog.com](http://www.analog.com).

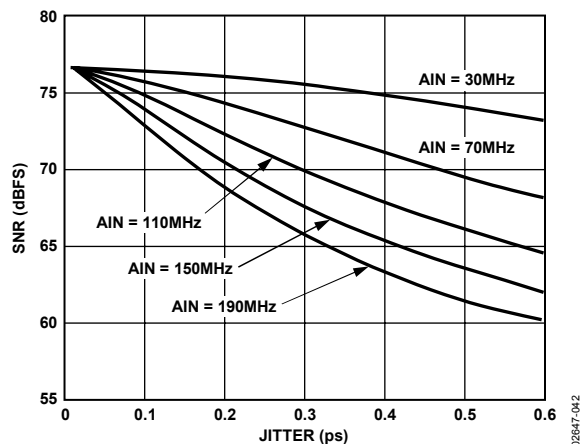


Figure 42. SNR vs. Jitter

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Table 8. AD6645/PCB Bill of Materials

Qty. 80 MSPS	Qty. 105 MSPS	Reference ID <sup>1</sup>	Description	Manufacturer	Supplier Part No.
1	1	PCB	Printed circuit board, AD6645 engineering evaluation board	PCSM	6645EE01D REV D
4	4	C1, C2, C31, C38	Capacitor, tantalum, SMT BCAPTAJC, 10 µF, 16 V, 10%	Kemet	T491C106K016AS
8	8	C3, C7 to C10, C16, C30 <sup>2</sup> , C32	Capacitor, ceramic, SMT 0508, 0.1 µF, 16 V, 10%	Presidio Components	0508X7R104K16VP3
9	9	C4, C15, C22 to C26, C29, (C33) <sup>3</sup> , (C34) <sup>3</sup> , C39	Capacitor, ceramic, SMT 0805, 0.1 µF, 25 V, 10%	Panasonic	ECJ-2VB1E104K
0	0	(C5, C6) <sup>3</sup>	Capacitor, ceramic, SMT 0805, 0.01 µF, 50 V, 10%	Panasonic	ECJ-2YB1H103K
10	10	C11 to C14, C17 to 21, C40	Capacitor, ceramic, SMT 0508, 0.01 µF, 50 V, 0.2%	Presidio Components	0508X7R103M2P3
0	0	(C27 to 28)	Capacitor, ceramic, SMT 0805, select		
1	1	CR1 <sup>3</sup>	Diode, dual Schottky HSMS2812, SOT-23, 30 V, 20 mA	Panasonic	MA716-(TX)
1	1	E1	Install jumper (across OPT_LAT and BUFLAT)		
5	5	F1 to F5	EMI suppression ferrite chip, SMT 0805	Steward	HZ0805E601R-00
1	1	J1	Header, 6-pin, pin strip, 5 mm pitch	Wieland	Z5.530.0625.0
1	1	J1	Pin strip, 6-pin, 5 mm pitch	Wieland	25.602.2653.0
1	1	J2	Header, 40-pin, male, right angle	Samtec	TSW-120-08-T-D-RA
2	2	(J3), J4, J5	Connector, gold, male, COAX-, SMA, verticle	Johnston Components™	142-0701-201
1	1	L1	Inductor, SMT, 1008-ct package, 4.7 nH	Coilcraft®	1008CT-040X-J
0	0	(R1) <sup>3</sup>	Resistor, thick film, SMT 0402, 100 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF1000V
0	0	(R2)	Resistor, thick film, SMT 1206, 60.4 Ω, 1/8 W, 1%	Panasonic	ERJ-8ENF60R4V
2	2	(R3 to 5) <sup>2</sup> , (R8) <sup>2</sup> , R9, R10	Resistor, thick film, SMT 0805, 500 Ω, 1/10 W, 1%	Panasonic	ERJ-6ENF4990V
2	2	R6 to R7	Resistor, thick film, SMT 0805, 25.5 Ω, 1/10 W, 1%	Panasonic	ERJ-6ENF25R5V
0	0	(R11) <sup>3</sup> , (R13) <sup>3</sup>	Resistor, thick film, SMT 0805, 66.5 Ω, 1/10 W, 1%	Panasonic	ERJ-6ENF66R5V
0	0	(R12) <sup>3</sup> , (R14) <sup>3</sup>	Resistor, thick film, SMT 0805, 100 Ω, 1/10 W, 1%	Panasonic	ERJ-6ENF1000V
1	1	R15 <sup>2</sup>	Resistor, thick film, SMT 0402, 178 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF1780X
1	1	R35	Resistor, thick film, SMT 0805, 49.9 Ω, 1/10 W, 1%	Panasonic	ERJ-6ENF49R9V
4	4	RN1 to RN4	Resistor array, SMT 0402; 100 Ω; 8 ISO RES., 1/4 W; 5%	Panasonic	EXB2HV101JV
2	2	T2 <sup>3</sup> , T3 <sup>2</sup>	Transformer, ADT4-1WT, CD542, 2 MHz to 775 MHz	MiniCircuits	ADT4-1WT
1	0	U1	IC, 14-bit, 80 MSPS ADC, QFP-52	Analog Devices	AD6645ASQ-80
0	1	U1	IC, 14-bit, 105 MSPS ADC, QFP-52	Analog Devices	AD6645ASQ-105
2	2	U2, U7	IC, SOIC-20, OCTAL D-type flip-flop	Fairchild	74LCX574WM
0	0	(U3) <sup>2</sup>	IC, SOIC-8, low distortion differential ADC driver	Analog Devices	AD8138ARM
2	2	U4, U6	IC, SOT-23, tiny logic UHS 2-input or gate	Fairchild	NC7SZ32
0	0	(U8) <sup>3</sup>	IC, SOIC-8, differential receiver	Motorola	MC100EL16
1	0	Y1	Clock oscillator, 80 MHz	CTS Reeves	MX045-80
4	4	Y1	Pin sockets, closed end	AMP	5-330808-3
4	4		Circuit board support	RICHO	CBSB-14-01

<sup>1</sup> Reference designators in parentheses are not installed on standard units.

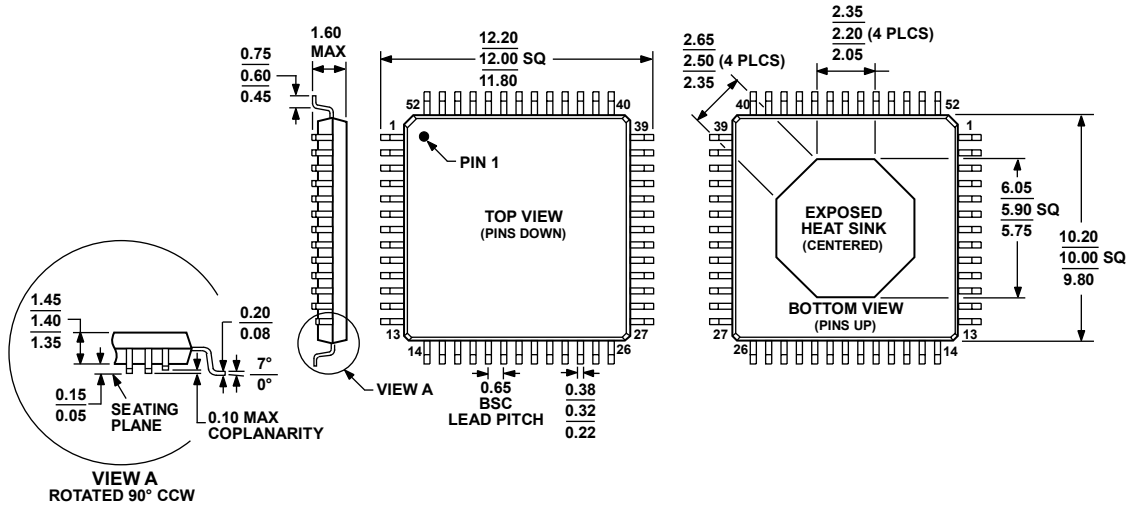
<sup>2</sup> AC-coupled AIN is standard: R3, R4, R5, R8, and U3 are not installed. If dc-coupled AIN is required, C30, R15, and T3 are not installed.

<sup>3</sup> AC-coupled encode is standard: C5, C6, C33, C34, R1, R11 to R14, and U8 are not installed. If PECL encode is required, CR1 and T2 are not installed.





OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BCC-HD  
 Figure 48. 52-Lead Low Profile Quad Flat Package, PowerQuad [LQFP\_PQ4]  
 (SQ-52-1)  
 Dimensions shown in millimeters

110308-A

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6645ASQ-80	-40°C to +85°C	52-Lead Low Profile Quad Flat Package, PowerQuad (LQFP_PQ4)	SQ-52-1
AD6645ASQZ <sup>1</sup> -80	-40°C to +85°C	52-Lead Low Profile Quad Flat Package, PowerQuad (LQFP_PQ4)	SQ-52-1
AD6645ASQ-105	-10°C to +85°C	52-Lead Low Profile Quad Flat Package, PowerQuad (LQFP_PQ4)	SQ-52-1
AD6645ASQZ <sup>1</sup> -105	-10°C to +85°C	52-Lead Low Profile Quad Flat Package, PowerQuad (LQFP_PQ4)	SQ-52-1
AD6645-80/PCB		Evaluation Board	
AD6645-105/PCB		Evaluation Board	

<sup>1</sup>Z = Pb-free part.

**AD6645**

**NOTES**